IN THE CLAIMS:

Please write the claims to read as follows:

1-66. (Canceled).

67. (Currently Amended): A processor, comprising:

a first execution unit having a first and second input register coupled to first and second inputs to a first arithmetic logic unit (ALU), the first and second input registers of the first execution unit to store source operands;

a second execution unit having a first and second input register, the second register coupled to a second input to a second ALU, the first and second input registers of the second execution unit to store source operands; and

a multiplexer ~~mulitplexer~~ (MUX) having i) a first input coupled to the first input of the first ALU, ii) a second input coupled to the first input register of the second ALU, and iii) an output directly providing a first input to the second ALU, the MUX permitting both the first and second ALU to share the source operand stored in the first input register of the first ALU.

68. (Previously Presented): The processor of claim 67, further comprising:

an instruction set defining a register decode value that specifies source operand bypassing, such that the MUX, in response to the register decode value that specifies source operand bypassing, selects the first input of the MUX coupled to the first input of the first ALU as the output of the MUX, the output of the MUX providing the first input to the second ALU.

69. (Previously Presented): The processor of claim 68, wherein the source operand bypassing value allows the second execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first execution unit.

70. (Previously Presented): The processor of claim 67, further comprising:

a local bus for communicating with a memory;

a register file for storing intermediate operands; and

an instruction decode stage for coupling the register file to the first and second input registers of the first and second ALUs to provide intermediate operands as the source operands, and for coupling a memory bus to the first input register of the of the first ALU to provide source operands from the memory.

71. (Previously Presented): The processor of claim 70, wherein the first input register of the first ALU provides source operands from the memory to both the first input to the first ALU and to the first input of the MUX, thereby permitting the first input to the second ALU to share the source operands from the memory directly from the first input register of the first ALU.

72. (Previously Presented): The processor of claim 67, further comprising:

a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback, and execution stages, the execution stage having the first and second execution units.

73. (Previously Presented): The processor of claim 72, further comprising:

an instruction set defining a register decode value that defines result bypassing that allows bypassing of a result from a previous instruction executing in pipeline stages of the processor by directly addressing a result register of the first and second execution units.

74. (Previously Presented): The processor of claim 73, wherein the register decode value comprises:

one of a result bypass (RRB) operand and an inter-unit result bypass (RIRB) operand, each of which explicitly controls data flow within the pipeline of the processor.

75. (Previously Presented): The processor of claim 74, wherein the RRB operand denotes the first execution unit and the RIRB operand denotes the second execution unit.

76. (Previously Presented): The processor of claim 74, wherein the RRB operand explicitly infers feedback of the data delivered from the first execution unit to an input register of the first execution unit over a feedback path.

77. (Previously Presented): The processor of claim 76, wherein the writeback stage comprises an interstage register and wherein the RRB operand enables bypassing write-back of the data processed by the first and second execution units to one of the register file or the interstage register of the writeback stage.

78. (Previously Presented): The processor of claim 67, further comprising:

an instruction set defining a register decode value that defines source operand bypassing that allows source operand data to be shared among the first and second execution units by directly addressing a source register of the first execution unit.

79. (Previously Presented): The processor of claim 78, wherein the source operand bypassing value allows the second execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first execution unit.

80. (Previously Presented): The processor of claim 67, further comprising:

a register file containing a plurality of general-purpose registers for storing intermediate result data processed by the first and second execution units.

81. (Previously Presented): The processor of claim 67, wherein the first and second execution units are parallel execution units.

82. (Previously Presented): The processor of claim 67, further comprising:

a current execution unit as the first execution unit; and

an alternate execution unit as the second execution unit.

83. (Previously Presented): The processor of claim 67, wherein the first and second ALU share the source operand stored in the first input register of the first ALU substantially simultaneously.

84. (Currently Amended): A processor, comprising:

a first arithmetic logic unit (ALU);

a second ALU;

a multiplexer ~~mulitplexer~~ (MUX) having i) a first input coupled to a first input of the first ALU, ii) a second input coupled to source operands, and iii) an output providing a first input to the second ALU, the MUX permitting both the first and second ALU to share the same source operand; and

an instruction set defining an instruction that when decoded operates the MUX to permit both first and second ALUs to share the same source operand.

85. (Previously Presented): The processor of claim 84, further comprising:

a local bus for communicating with a memory, wherein the first and second ALUs share the same source operand from memory.

86. (Previously Presented): The processor of claim 84, further comprising:

a register decode value of the instruction set that defines source operand bypassing that allows source operand data to be shared among the first and second ALUs by directly addressing a source register of the first ALU.

87. (Previously Presented): The processor of claim 86, wherein the source operand bypassing value allows the second ALU to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first ALU.

88. (Previously Presented): The processor of claim 84, further comprising:

a register file containing a plurality of general-purpose registers for storing intermediate result data processed by the first and second ALUs.

89. (Previously Presented): The processor of claim 84, wherein the first and second ALUs are parallel ALUs.

90. (Previously Presented): The processor of claim 84, further comprising:

a current ALU as the first ALU; and

an alternate ALU as the ALU unit.

91. (Previously Presented): The processor of claim 84, wherein the first and second ALUs share the same source operand substantially simultaneously.

92. (Currently Amended) A method for use with a processor, the method comprising:

providing a multiplexer ~~mulitplexer~~ (MUX) having a first and second MUX input and a MUX output;

coupling the first MUX input to a first input of a first ALU;

coupling a second MUX input to a first input register of a second ALU; and

directly providing, by the MUX output, a first input to the second ALU, the MUX permitting both the first and second ALU to share a source operand stored in a first input register of the first ALU.

93. (Previously Presented): The method of claim 92, further comprising:

defining a register decode value within an instruction set that specifies source operand bypassing, such that the MUX, in response to the register decode value that specifies source operand bypassing, selects the first MUX input coupled to the first input of the first ALU as the MUX output, the MUX output providing the first input to the second ALU.

94. (Previously Presented): The method of claim 93, wherein the source operand bypassing value allows the second execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first execution unit.

95. (Previously Presented): The method of claim 92, further comprising:

communicating with a memory;

storing intermediate operands in a register file; and

identifying an instruction decode stage for coupling the register file to the first and second input registers of the first and second ALUs to provide intermediate operands as source operands, and for coupling a memory bus to the first input register of the of the first ALU to provide source operands from the memory.

96. (Previously Presented): The method of claim 95, further comprising:

providing, by the first input register of the first ALU, source operands from the memory to both the first input to the first ALU and to the first MUX input, thereby permitting the first input to the second ALU to share the source operands from the memory directly from the first input register of the first ALU.

97. (Previously Presented): The method of claim 92, further comprising:

including a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback, and execution stages, the execution stage having a first and second execution unit, each having one of the first and second ALUs, respectively.

98. (Previously Presented): The method of claim 97, further comprising:

defining a register decode value that defines result bypassing of a result from a previous instruction executing in pipeline stages of the processor.

99. (Previously Presented): The method of claim 98, further comprising:

identifying a pipeline stage register for use as a source operand in an instruction containing the register decode value by directly addressing a result register.

100. (Previously Presented): The method of claim 99, further comprising:

explicitly controlling data flow within the pipeline stages of the processor through the use of a register result bypass (RRB) operand in the register decode value.

101. (Previously Presented): The method of claim 100, wherein the step of explicitly controlling comprises:

retrieving data from the first execution unit; and

returning the data to an input of the first and second execution units as specified by the RRB operand, thereby bypassing write-back of the data to either a register file or memory at the writeback stage.

102. (Previously Presented): The method of claim 101, wherein the step of identifying further comprises:

explicitly specifying the pipeline stage register to be used as the source operand for the instruction.

103. (Previously Presented): The method of claim 102, further comprising:

encoding the RRB operand in fewer bits than a regular register operand.

104. (Previously Presented): The method of claim 97, further comprising:

defining a register decode value that defines source operand bypassing of source operand data.

105. (Previously Presented): The method of claim 104, further comprising:

identifying a pipeline stage register for use as a source operand in an instruction containing the register decode value by directly addressing a source register.

106. (Previously Presented): The method of claim 105, further comprising:

sharing source operand data among the first and second execution units of the pipelined processor through the use of a source bypass (RISB) operand in the register decode value.

107. (Previously Presented): The method of claim 106, wherein the step of sharing further comprises:

receiving data at the second execution unit, the data stored at a memory address specified by a displacement operand in a previous instruction executed by the first execution unit of the processor.

108. (Previously Presented): The method of claim 107, wherein the step of sharing further comprises:

realizing two memory references through the use of a single bus operation over a local bus.

109. (Previously Presented): The method of claim 108, wherein the step of sharing further comprises:

encoding the RISB operand with substantially fewer bits than those needed for a displacement address.

110. (Previously Presented): The method of claim 92, further comprising:

sharing a source operand stored in a first input register of the first ALU at the first and second ALU substantially simultaneously.

111. (Currently Amended) An apparatus, comprising:

means for providing a multiplexer ~~mulitplexer~~ (MUX) having a first and second MUX input and a MUX output;

means for coupling the first MUX input to a first input for a first ALU;

means for coupling a second MUX input to a first input register for a second ALU; and means for directly providing, by the MUX output, a first input to the second ALU, the MUX permitting both the first and second ALU to share a source operand stored in a first input register of the first ALU.

112. (Previously Presented): The apparatus of claim 111, further comprising:

means for defining a register decode value within an instruction set that specifies source operand bypassing, such that the MUX, in response to the register decode value that specifies source operand bypassing, selects the first MUX input coupled to the first input of the first ALU as the MUX output, the MUX output providing the first input to the second ALU.

113. (Previously Presented): The apparatus of claim 112, wherein the source operand bypassing value allows the second execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the first execution unit.

114. (Previously Presented): The apparatus of claim 111, further comprising:

means for communicating with a memory;

means for storing intermediate operands; and

means for identifying an instruction decode stage for coupling the register file to the first and second input registers of the first and second ALUs to provide intermediate operands as source operands, and for coupling a memory bus to the first input register of the of the first ALU to provide source operands from the memory.

115. (Previously Presented): The apparatus of claim 114, further comprising:

means for providing, by the first input register of the first ALU, source operands from the memory to both the first input to the first ALU and to the first MUX input, thereby permitting the first input to the second ALU to share the source operands from the memory directly from the first input register of the first ALU.

116. (Previously Presented): The apparatus of claim 111, further comprising:

means for sharing a source operand stored in a first input register of the first ALU at the first and second ALU substantially simultaneously.

117. (Currently Amended) A computer readable media, comprising: the computer readable media containing instructions for execution in a processor for the practice of the method of,

providing a multiplexer ~~mulitplexer~~ (MUX) having a first and second MUX input and a MUX output;

coupling the first MUX input to a first input of a first ALU;

coupling a second MUX input to a first input register of a second ALU; and

directly providing, by the MUX output, a first input to the second ALU, the MUX permitting both the first and second ALU to share a source operand stored in a first input register of the first ALU.